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Pre-encoded Multiplier based on Non-Redundant RADIX-4 Signed Digit Encoding

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Abstract. Multiplier is a basic component for implementing computationally intensive applications. Multimedia and digital signal processing (DSP) applications (e.g., Fast Fourier transform (FFT), audio/video Codes) carry out a large number of multiplications with coefficients that do not change during the execution of the application. The research activities in the field of arithmetic optimization have shown that the design of arithmetic components combining operations which share data, can lead to significant performance improvements. Modified Booth (MB) encoding tackles the aforementioned limitations and reduces to half the number of partial products resulting to reduced area, critical delay and power consumption. However, a dedicated encoding circuit is required and the partial products generation is more complex. According to NR4SD except the most significant one that is MB encoded. In this paper, we introduce architecture of pre-encoded multipliers for Digital Signal Processing applications based on off line encoding of coefficients.
Index Terms. Signal processing, Carry save, FFT.

INTRODUCTION

The size of ROM used to store the groups of coefficients is significantly reduced as well as the area and power consumption of the circuit. We introduce architecture of pre-encoded multipliers introduced for digital signal processing applications based on off-line encoding of coefficients., is proposed leading to a multiplier design with less complex partial products implementation. Extensive experimental analysis verifies that the proposed pre-encoded NR4SD multipliers, including the coefficients memory, are more area and power efficient along with the conventional Modified Booth scheme.

The size of ROM used to store the groups of coefficients is significantly reduced as well as the area and power consumption of the circuit. However, this multiplier design lacks flexibility since the partial products generation unit is designed specifically for a group of coefficients and cannot be reused for another group. Also, this method cannot be easily extended to large groups of predetermined coefficients attaining at the same time high efficiency.

In order to cover the dynamic range of the 2's complement form, all digits of the proposed representation are encoded according to NR4SD except the most significant one that is MB encoded. Using the proposed encoding formula, we pre-encode the standard coefficients and store them into a ROM in a condensed form (i.e., 2 bits per digit). Compared to the pre-encoded MB multiplier in which the encoded coefficients need 3 bits per digit, the proposed NR4SD scheme reduces the memory size. Also, compared to the MB form, which uses five-digit values {-2, -1, 0, +1, +2}, the proposed NR4SD encoding uses four-digit values. Thus, the NR4SD-based pre-encoded multipliers include a less complex partial products generation circuit. We explore the efficiency of the aforementioned pre-encoded multipliers considering the size of the coefficients ROM.

LITERATURE SURVEY

Modified Booth is a redundant radix-4 encoding technique. Considering the multiplication of the 2's complement numbers A, B, each one consisting of n = 2k bits, B can be represented in MBform as:

$B = (b_{n-1}\ldots\ldots b_0)_{2's} = -b_{2k-1}2^{2k-1} + \sum_{i=0}^{2K-2} b^i 2^i$

$= (b_{k-1}{}^{MB}\ldots\ldots b_0{}^{MB})_{MB} = \sum_{j=0}^{K-1} b^{MB} 2^{2j}$

Digits $b^{MB} \in \{-2, -1, 0, +1, +2\}$, $0 \le j \le k-1$, are formed as follows:

$$b^{MB}_j = -2b_{2j+1} + b_{2j} + b_{2j-1}$$

Where $b_{-1} = 0$. Each MB digit is represented by the bits s, one and two. The bit s shows if the digit is negative (s = 1) or positive (s = 0). One shows if the absolute value of a digit equals 1(one = 1) or not (one = 0). Two shows if the absolute value of a digit equals 2 (two = 1) or not (two = 0). Using these bits, we calculate the MB digits b^{MB}_j as follows:

$$b^{MB}_j = (-1)^{sj} .(onej + 2twoj)$$

Equations (4) form the MB encoding signals. .

Sj= b2j+1, onej = b2j-1 ^ b2j;
twoj = (b2j+1 ^ b2j) ^ (~onej);

0	0	0	0	0	0
0	0	1	+1	0	1
0	1	0	+1	0	1
0	1	1	+2	0	0
1	0	0	−2	1	0
1	0	1	−1	1	1
1	1	0	−1	1	1
1	1	1	0	1	0

Table 1: Modified Booth Encoding

The architecture system design comprises the conventional MB multiplier and the ROM with coefficients in 2's complement form. Let us consider the multiplication A and B. The coefficient B = $(b_{n-1}\ldots\ldots b_0)_{2's}$ consists of n = 2k bits and is driven to the MB encoding blocks from a ROM where it is stored in 2's complement form. It is encoded according to the MB algorithm and multiplied by A= $(a_{n-1}\ldots\ldots a_0)_{2's}$, which is in 2's complement representation. We note that the ROM data bus width equals the width of coefficient B (n bits) and that it outputs one coefficient on each clock cycle.

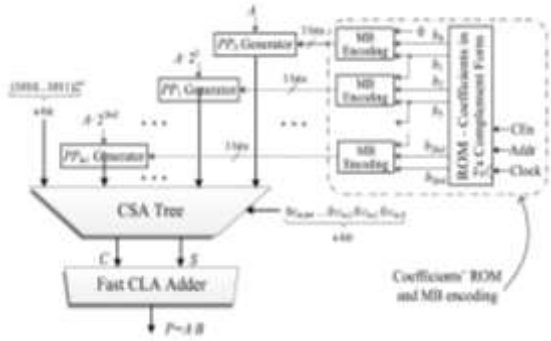

Fig.1. Architecture of modified booth multiplier design

PROPOSED WORK

The proposed Modified Booth is a redundant radix-4 encoding technique. Each MB digit is represented by the bits, one and two. The bits show if the digit is negative (s = 1) or positive (s = 0). One shows if the absolute value of a digit equals 1 (one = 1) or not (one = 0). Two shows if the absolute value of a digit equals 2 (two = 1) or not (two = 0).

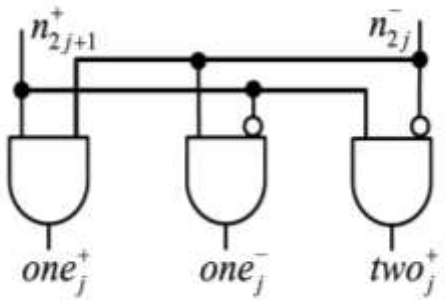

Fig.2. Encoding of booth multiplier

The output of the PPG circuit is again given as an input for CSA (Carry Save Adder) Tree. The carry-save output of the CSA tree is finally summed using a fast CLA adder. The CSA tree and CLA adder were imported from Synopsys Design Ware library. The ROM for the 2's complement or pre-encoded coefficients is a synchronous ROM of 512 words often met at DSP systems, e.g., speech Codecs or audio filtering. The width of each ROM depends on the multiplier architecture.

RESULTS

In this project, the proposed designed was developed. These all blocks are designed using Verilog HDL. The RTL description is synthesized and simulated in Xilinx ISE 14.5. The simulated wave forms are presented below

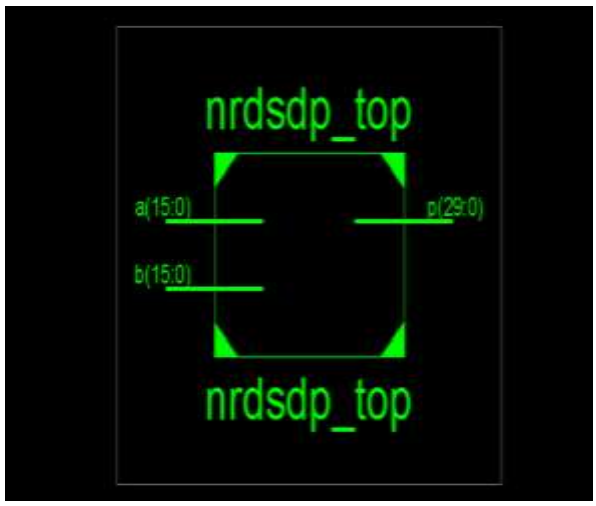

Fig.3. Top level schematic diagram

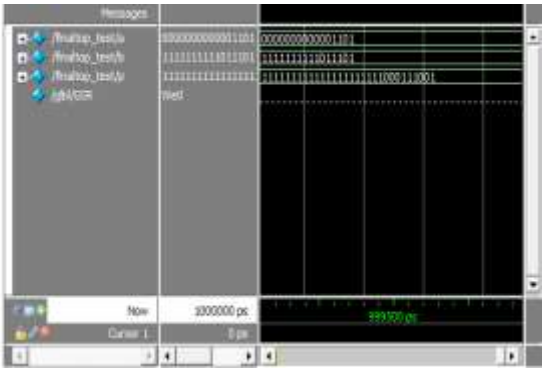

Fig.4. Wave form of multiplier

SUMMARY AND CONCLUSION

A new design of multipliers is explored by off-line encoding the standard coefficients and storing them in system memory. The proposed multiplier designs are more area and power efficient compared to the conventional MB designs. Synthesis and Simulation analysis in Xilinx 14.5 software using Verilog Hardware Description Language verifies the gains of the proposed multipliers in terms of area complexity and power consumption compared to the conventional MB multiplier.

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